

# **Design of the Basic Engineering Project subject for the second year of Electrical Engineering at Telecom BCN**

**Ramon Bragós**

Telecom BCN, Electronics Engineering department, UPC, Barcelona, Spain

**Eduard Alarcón**

Telecom BCN, Electronics Engineering department, UPC, Barcelona, Spain

**Josep Pegueroles**

Telecom BCN, Telematics department, UPC, Barcelona, Spain

**Adriano Camps**

Telecom BCN, Signal Theory and Communications department, UPC, Barcelona, Spain

**Albert Oliveras**

Telecom BCN, Signal Theory and Communications department, UPC, Barcelona, Spain

**Miguel García-Hernández**

Telecom BCN, Electronics Engineering department, UPC, Barcelona, Spain

**Elisa Sayrol**

Telecom BCN Dean, Signal Theory and Communications dept, UPC, Barcelona, Spain

## **ABSTRACT**

The Basic Engineering Project is a second year subject which represents the second of four steps in the design-implement subjects path of the Telecom BCN curricula. The first one is included into the Introduction to Engineering subject and the last one is the degree Thesis. While the first and third year projects have a wide scope (from client specification to business idea), the second year project emphasizes on the technical design, implementation and characterization of a given block from its specifications but understanding the whole system concept and has a higher technical difficulty. A complex ICT system is split in blocks. All students should know the block structure but a given work team will only develop one of the system blocks. The structure of laboratory groups allows that students could select the block according to the major they will choose the following year (electronics, networks, audiovisual systems and communications). The course structure design includes three initial sessions oriented to provide disciplinary contents related with the project topic using the puzzle methodology. Then the block to be designed is fully specified and documented in the Requirements Specification document. The following 10 sessions are devoted to the design, prototyping and validation of the chosen system block. Their schedule is determined by the time plan and work package organisation that the work teams prepare and write in the Project Plan document. The preliminary and critical design reviews are performed during two progress meetings in the 7<sup>th</sup> and 11<sup>th</sup> week. This first year of implementation, the product to be designed, that has been divided in blocks is an in-home audio system component. Given that the course is running this first year with a pilot group of 24 students, only the amplifier and preequalizer blocks have been designed and built by the students.

## KEYWORDS

Design-build subject, Electronic Engineering, Audiovisual Engineering, Project-based Learning.

## INTRODUCTION: THE DESIGN-BUILD SUBJECTS PATH AT TELECOM-BCN

Five new bachelor degrees (4 year-long) have started this 2010-2011 academic year at Telecom BCN, the Electrical and Telecom Engineering School of the Technical University of Catalonia (UPC). Two of them (Audiovisual Systems Engineering and Electronics Engineering) already started the last academic year as pilot courses and the remaining three degrees (Communication Systems Engineering, Networks, and Telecom Science and Technology) are now running the second semester.

According to the CDIO Standards, we designed the curricula structure using a mixed approach to integrate CDIO skills into the curricula: On the one hand, the skills pathways were defined by involving all courses. Every course may contribute to the learning of several skills at a given level (basic, medium, advanced) and should actively contribute to develop and assess two of them. On the other hand, four specific project-centered courses have been scattered along the curricula, at the second semester of each academic year. They all include design-build activities and put emphasis on the CDIO Syllabus fourth group of skills. Table 1 shows their main characteristics.

Table 1  
Project subjects along the curriculum

Subject	Semester	Credits (hours)	Main topics and characteristics	Group size
Introduction to Engineering	2	6 (150)	System view Basic economics Project management Seminars Partially guided project (2.4 ECTS)	4
Basic Engineering Project	4	6 (150)	Regulatory aspects of ICT (2 ECTS) Open basic engineering project (4 ECTS) Focus on design and implementation of a given block of a complex system	4-6
Advanced Engineering Project	6	12 (300)	Seminars (< 20%) Whole design and implementation of an advanced and complex engineering project Different topic per group Focus on conception, innovation and entrepreneurship	9-12
Thesis project	8	24 (600)	Individual (by Spanish law) Performed in a company or research group, on campus or in an international exchange.	1

Last academic year, 56 students from the two pilot degrees followed the *Introduction to Engineering* subject. The experience was reported in the 2010 CDIO Conference [1]. This year, 240 students are running it. Meanwhile, 24 students from the first cohort are taking the pilot course of the second design-build subject, the *Basic Engineering Project*.

The scope balance of the design-build subjects of the first three years is similar to that reported in [2], although the implementation of the first year project is quite different. The scopes of the first and third projects are wide while the second one is narrower. The depth, of course, increases each year. In the next figure, the scope of the three project subjects is displayed under the LIPS project cycle representation [3]:

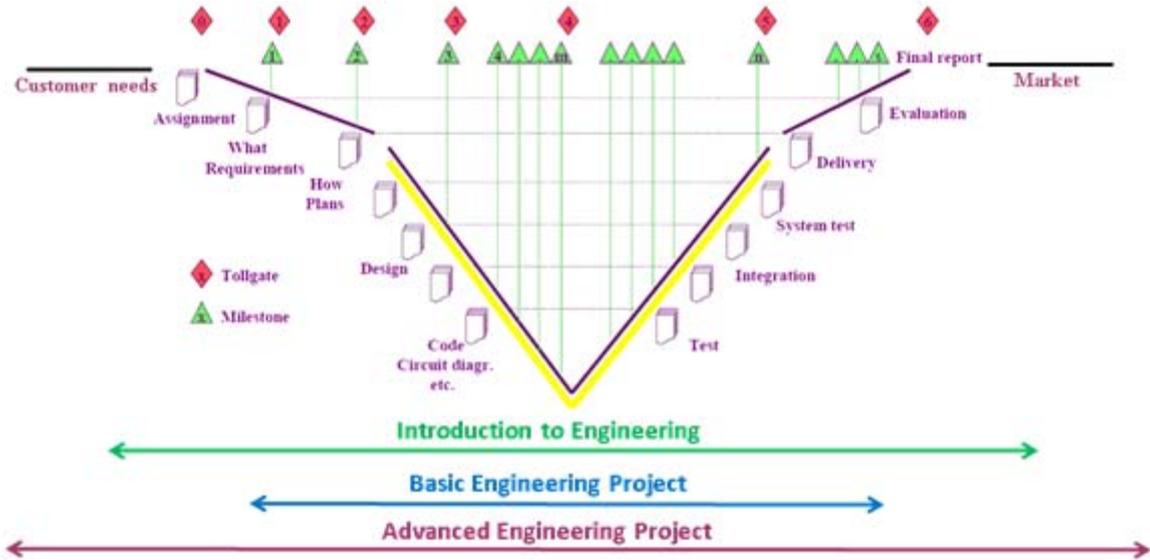


Figure 1. Scope of the three first design-build subject projects represented below the LIPS project cycle representation (adapted from [3]).

The project included in the Introduction to Engineering subject is partially guided and has low complexity, but has a broad scope, given that the students start from a system-level client specifications, they design parts of the system, build the whole system and should define a business idea based on a similar device. On the other hand, the second year project (Basic Engineering Project) has a higher technical difficulty and emphasizes the modular structure of complex ICT systems, although a work team will only develop one of the system blocks. The product is defined by the client (faculties) and also the block breakdown is given. The student teams should design and implement only a given block from specifications but knowing the whole system structure and the interfaces between blocks. The final result is delivered to the company internal client (again the faculties). In the third year project (Advanced Engineering Project), larger work groups would develop a whole system, including its business plan. They should conceive the product, define the project breakdown structure and work packages, distribute them between the sub-teams, design and implement the sub-systems, integrate them and define a business plan based on the product. That is, to take the broad scope of the first project together with the depth of the second and the business and management concepts learnt in a specific subject which is located in the first half of the third year. The Advanced Engineering Project subject has not yet been implemented. It will be done in the second half of the 2011-2012 academic year.

**THE BASIC ENGINEERING PROJECT SUBJECT**

**Course structure**

Two of the six ECTS credits are used to learn the contents and practical aspects on the regulation of telecommunications, which is required for the professional ICT engineering practitioners in Spain. The Basic Engineering Project is performed in the remaining 4 ECTS

credits (3 hours/week in the lab + 4 hours/week of autonomous work). It can be argued that a reasonable way to arrange this double function of the subject would have been to include the regulatory aspects in the projects. This is true, but this solution drives to the need of performing strict telecommunication facilities projects with all students, while the adopted solution allows us to choose a wider range of topics. With the selected way, if a given set of students choose an advanced project on telecom facilities, they would learn more about regulatory contents, but all students have received the minimum mandatory training.

There is a constraint due to the structure of our curricula: the students of electrical engineering are attending their second year, which is common to all of them, but they are going to split in four majors in the third year: electronics, audiovisual systems, networks and telecommunication systems (there is an additional degree, which has a wider scope, Telecom Science and Technology). Then, the students' interests can be slightly different. A whole system would include aspects from all these specialities, but not a given block. Then, there is a trade-off between the depth and breadth of the design given the limited time schedule (4 ECTS credits). To solve this compromise, we have designed a course structure where the students will be allowed to choose which part of the system would develop. A given system (figure 2) is divided in four blocks including aspects of hardware development, communications, network protocols and audio/image/video signal processing. Given that the second year students are mixed in class groups, we should give simultaneous labs with support of lecturers from different departments (figure 3)

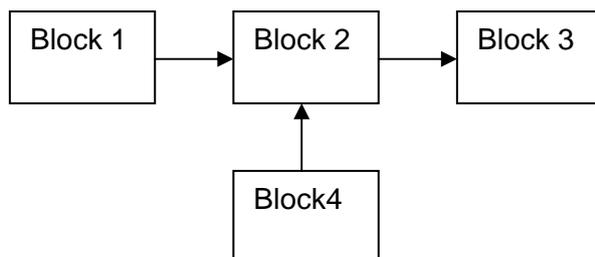


Figure 2: System block diagram

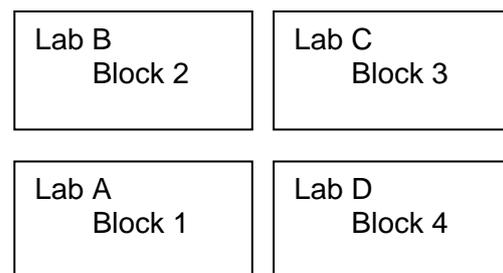


Figure 3: Simultaneous labs structure

Students can be grouped together to make the project according to their specialty although they are mixed up in class. Two class groups (60-80 students) would give enough diversity to fill the four sub-projects. Variations in the technology used to implement each block can drive to different projects built around an initial proposal, which allows amortizing the effort made by the faculties when designing the case study and use it along 2-4 semesters.

### **Course goals and learning outcomes**

Course goals:

- Consolidation and improvement of the learning outcomes of previous and simultaneous courses
- Enhancement of the CDIO skills at medium level (mainly Design and Implementation)
- Acquisition of generic skills at medium level (see table 2)

Learning outcomes:

- Project management and documentation skills
- Specific disciplinary knowledge about the project topic
- Practical design and implementation skills
  - System and circuit level simulation and characterization
  - Measurement strategies
  - Electronic components selection and circuit building
- Generic skills learning outcomes (assigned and defined in the degree syllabus)

Table 2  
Generic skills (medium level) stressed and assessed in this course

#	Generic Skill	Exposed	Stressed	Assessed
1	Innovation and entrepreneurship	X	X	X
2	Societal and environmental context	X	X	X
3	Communication in a foreign language (English)	X	X	
4	Oral and written communication	X	X	X
5	Teamwork	X	X	
6	Survey of information resources	X	X	
7	Autonomous learning	X		
8	Ability to identify, formulate and solve engineering problems	X		
9	Ability to Conceive, Design, Implement and Operate complex systems in the ICT context	X	X	X
10	Experimental behaviour and ability to manage instruments	X	X	

### **Course design**

The students are grouped in teams of 4-6 (depending on the project complexity) and sign a team constitution agreement in which they define their role and commit to have a common ambition of reaching a given mark (pass, good, outstanding). A major concern we have had in the course design is the interpretation and application of the PBL methods to the course design. Leaving apart the classical concept of the “project subject” in the Spanish Engineering Schools, centred in the formal aspects (documentation, budget, ...) and not in creativity and design, the current trends (at least in Spain) are emphasizing the capability of PBL to improve the disciplinary contents learning instead of providing authentic engineering experiences. Of course, any implementation of PBL is better for the learning of skills than a classical expository course approach but, if a project subject is substituting a given disciplinary subject, the need of providing disciplinary contents drives to the use of contents-oriented methods (puzzles, lectures) which are a bit artificial in a real engineering context. On the other hand, these methods provide ways to assess the individual task of the students which are valuable. In our case, the project subjects are not substituting the disciplinary subjects but supporting them. Looking for a trade-off, we have limited to the first three sessions the disciplinary contents upgrading activities and left the remaining 10 sessions for design-build activities. The generic course schedule is shown in the following table. In the Course Implementation section, more details can be found over the example implemented this year.

Table 3  
Generic course schedule

Week	Activity	Deliverables
1	- Course introduction - Brainstroming about the product structure and specs. - Puzzle assignment	
2-3	- Puzzle activities about disciplinary contents referred to the project - Block requirements definition	1-2 pages report + 2 slides on each puzzle topic
4	- 3d puzzle about block implementation alternatives - Brainstroming about tasks and work packages planning	Requirement Specification document
5 -8	- Block design and prototyping	Project Plan document Prototype characterization
9-12	- Block improvement and finishing	Second prototype design
13	- Final project presentation	Project final report

The documentation has been adapted from the LIPS standard [3]. We started using the LIPS documents in the Introduction to Engineering subject project as they are. After two semesters, we find them a bit complex for small projects and we have simplified the structure of the documents, which are limited to: Requirement Specification, Project Plan, Progress Reports and Final Report.

**Course assessment**

The initial individual assignments have a small weight in the mark but it is mandatory to deliver them on time. There is a strong penalty (20% per delayed delivery) if less than 80% are delivered on time. Another 20% of the mark is obtained from individual tests about the project contents. The remaining 60% of the mark is assigned to the whole team performance, but there is a 10% which comes from the coherence in the individual marks of the team members, to promote the individual effort. The assessment of the deliverables is based on rubrics which try to take into account both the results and the procedures employed by the students.

- Puzzle and project individual assignments.....20%  
(20% penalty in the whole mark if less than 80% on time)
- Project .....60%
  - 20% half course performance
  - 30% final performance
  - 10% group coherence
- Project contents individual tests (2).....20%

**Course implementation**

This year, the chosen topic is the design of a component of an in-home audio system, an active loudspeaker able to be powered from the mains AC supply and which would play sound coming from a digital source transmitted wirelessly (figure 4).



Figure 4: Product definition: In-home audio system with wireless digital data streaming

The system blocks are: a) signal codification-decodification and streaming, b) transmission (wifi/zigbee/plc), c) amplification and d) digital equalization.

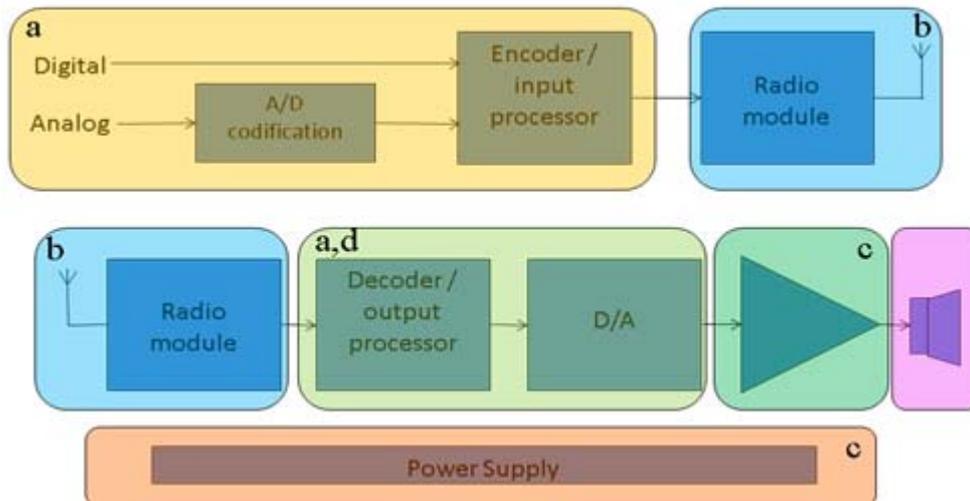


Figure 5: Product block structure and grouping of blocks in sub-projects

This first year of implementation we are running with a small pilot group of 24 students from electronic engineering and audiovisual systems engineering. Because of this, the system structure and blocks a) and b) are provided by the faculties. The students should design and build the amplifier, characterize it and also the amplifier-loudspeaker set behaviour and pre-equalize the whole response using Matlab. They have a restriction in cost and in power efficiency (>80%) so they are compelled to choose a D-class switched amplifier structure. Although this amplifier admits a complex implementation and analysis, it can also be understood by sophomore students [4]. The students have completed or are studying two courses on electronic circuits, signal processing and networks. They can only use the basic circuit blocks they know: operational amplifiers, comparators, transistors and filters. The design and implementation includes the following tasks:

- choosing the topology
- designing its main parameters
- simulating its behavioral model
- implementing the circuit blocks
- characterizing them separately and put together
- designing and building the printed circuit board
- characterizing the amplifier-loudspeaker set
- designing the digital equalizer
- characterizing the whole set
- side aspects: selecting a power supply, taking care of electromagnetic interferences.

The first day, after the course introduction, a brainstorming about the product structure and specifications was conducted. Then, the product block breakdown and interface properties were presented by the faculties and the assignment for this year (amplifier + pre-equalization) was established. The first sessions puzzles have been about audio amplifier structures: the topics have been split in four packages and prepared each one by one of the group members. The first puzzle (second day) was about audio amplifier classes: A, B, A-B, D. The second day, after the experts meeting and the presentation to the group partners, a brainstorming was conducted to extract the conclusions and to drive to the need of choosing a class-D structure after specifying a power efficiency higher than 80%. The second puzzle topics were: Class-D topologies, signal spectrum, output stages and output filters. After the second puzzle activities, the third day, a third brainstorming about pros and cons of the design alternatives was conducted. A third puzzle-like activity was proposed to give individual assignments for the preparation of the Matlab scripts that would be used to perform the behavioural simulation of the amplifier structure. At this point, the assignment for each group was clear and they could prepare the Requirement Specification document with their own interpretation

of the given specification. This document includes a background section which is filled by joining and integrating the documents prepared to fulfil the puzzle assignments. Once validated the Requirement Specification, the groups are asked to present the project Plan Document, which includes a Time Plan and a Work Package description. The remaining project weeks, the groups are supposed to follow this plan and are checked at two points: the Preliminary Design Review (PDR), at week 7, when the first prototype should be working and the Critical Design Review (CDR), at week 11, when there is no return in the chosen alternatives and the second prototype should be working, including the pre-equalisation, and only finishing and improving activities should be running. Figure 6 shows the V diagram of the project and table 3 the tollgates. The V diagram shows two parallel groups of tasks because, additionally to the amplifier circuit, they should design two Matlab based virtual instruments (frequency response analyser and audio spectrum analyser + THD measurer)

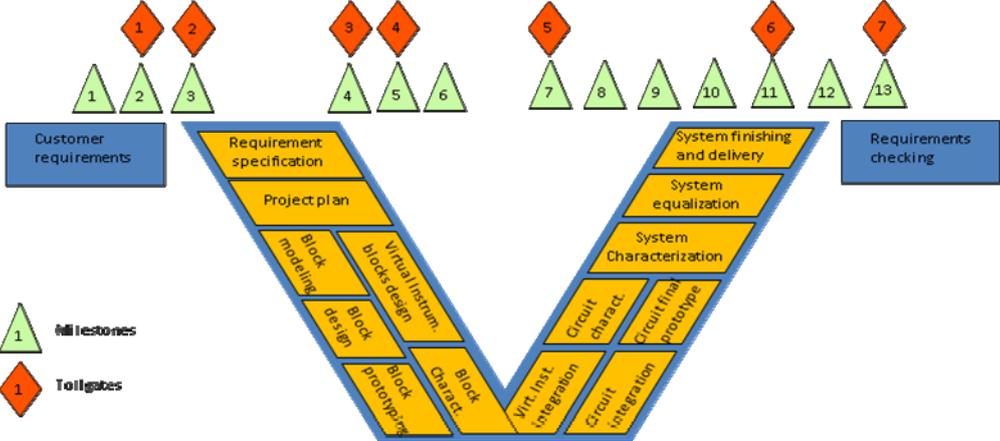


Figure 6: V diagram of the project. While the tollgates are determined by the faculties, the weekly milestones are internal decisions of the groups, according to their project plan.

Table 3  
Project tollgates and the corresponding deliverables

#	week	Deliverables
1	2	Puzzle 1
2	3	Puzzle 2
3	4	Blocks models, requirement specification, timeplan proposal
4	5	Project plan
5	7	First prototype evaluation. Progress meeting 1. PDR
6	11	Preequalizer . Progress meeting 2. CDR
7	14	Final results presentation

The next academic year enough students will be enrolled in that course to perform the simultaneous design of all the different blocks of a complex system in different laboratory groups. In the second year project, the students work in depth in the design of a block of a complex system and acquire skills to face the design of a complete complex system in the third year project. The pilot group will reach this project in the next academic year.

## REFERENCES

- [1] Bragós R. Alarcón E. Camps A. Pegueroles J. Sardà J. and Sayrol E., Conceiving and designing an "Introduction to Engineering" course within the new curricula at Telecom BCN, UPC Barcelona. Proceedings of the 6th International CDIO Conference, École Polytechnique, Montréal, 2010.
- [2] Rouvrais S. Ormrod J. Landrac G. Mallet J. Gilliot J-M. Thepaut A. and Tremenbert P., "A mixed project-based learning framework: preparing and developing student competencies in a French Grande Ecole" European Journal of Engineering Education:Engineering Competencies. Vol. 31, 2006, pp 83-93.
- [3] Svensson T. and Krylander C., "The LIPS project model. Ver 1.0 " Linköping University,Sweden, 2004.
- [4] Trullemans Ch. Labrique F., "From KCL to Class D Amplifier". ISCAS 2008.

### **Biographical Information**

Ramon Bragós is associate professor at the Electronics Engineering Department of Technical University of Catalonia (UPC). His current research focuses on electrical impedance spectroscopy applications in biomedical engineering. He lectures at Telecom BCN, where he is the Associate Dean of Academic Innovation.

Eduard Alarcón is associate professor at the Electronics Engineering Department of UPC. His current research includes signal and energy processing on silicon. He lectures at Telecom BCN, where he is the USA-Liaison Adjunct to the Dean.

Adriano Camps is full professor at the Signal Theory and Communications department of UPC. His current research focuses in microwave remote sensing, with special emphasis in microwave radiometry by aperture synthesis techniques and remote sensing using signals of opportunity. He lectures at Telecom BCN.

Josep Pegueroles is associate professor at the Telematics department of UPC. His current research focuses security for multimedia networked services and secure group communications. He teaches at Telecom BCN.

Albert Oliveras is associate professor at the Signal Theory and Communications department of UPC. His current research focuses in nonlinear image and signal processing and mathematical morphology, and its applications to biological signal processing. He lectures at Telecom BCN.

Miguel García-Hernández is full professor at the Electronics Engineering Department of UPC. His current research focuses in non destructive techniques based on ultrasound and infrared spectroscopy. He lectures at Telecom BCN.

Elisa Sayrol is associate professor at the Signal Theory and Communications department of UPC. Her current research focuses on image and video analysis as well as image and video watermarking. She lectures at Telecom BCN where she is the Dean.

### **Corresponding author**

Ramon Bragos  
UPC – Technical University of Catalonia  
Campus Nord, B3. c/ Jordi Girona 1-3  
08034 Barcelona, Spain  
sotsdirlabs@etsetb.upc.edu